HIGH VOLTAGE POWER TRANSISTORS IN HIGH FREQUENCY SWITCHING POWER SUPPLIES

During the testing of a switching power supply prototype, or when evaluating alternative types of power switching transistors, one of the normal checks consists of measuring the collector voltage and current and comparing the case temperatures of the power transistors.

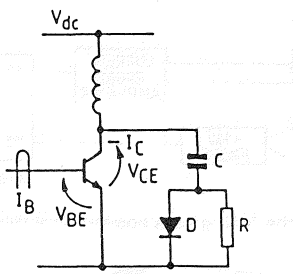
If the unit is to be reliable considering worst case operation, component tolerances and variations in transistor parameters a more detailed examination of the transistor drive and waveforms is needed. If this examination is made while deliberately 'degrading' the circuit it is also a very effective method of identifying potential points in the circuit design which may be critical. Also when comparing different types of switching transistor any which may be operating too close to their limits can be found.

It is often thought that power transistor failures in an SMPS are caused by voltage overstress. In most cases the design has allowed an adequate margin in selecting the devices voltage rating. Many failures in the laboratory, apart from the literal 'dropping of a spanner in the works', are more likely to be associated with current crowding problems which concentrate the power loss in a small area of the chip and lead to thermal failures.

The following suggestions are intended to illustrate the critical areas to look at and some simple ways to 'degrade' the circuit. Taking these results into consideration along with measurements of the case temperatures will enable the designer to select the appropriate devices for the application with confidence of their reliability in worst case situations.

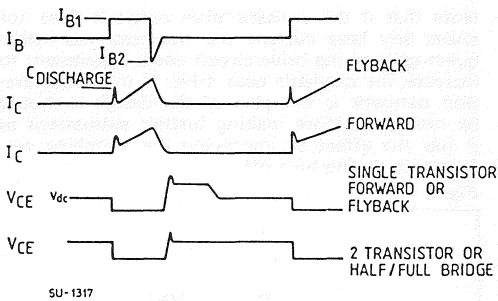
The basic circuit we are concerned with is:

Fig. 1



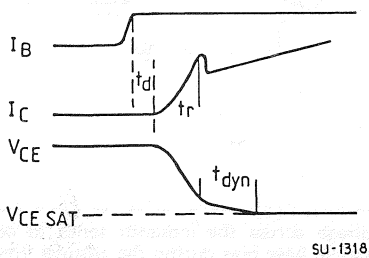
Typical waveforms associated with the main applications are:

Fig. 2



First the turn-on transition should be considered:

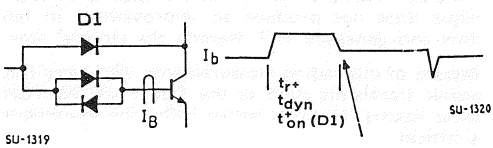
Fig. 3



Note that oscilloscope amplifier saturation makes it difficult to look carefully at t_{dyn} or $V_{CE(sat)}$.

However these parameters can be evaluated by adding an antisaturation network, if not already present. In this case we see:

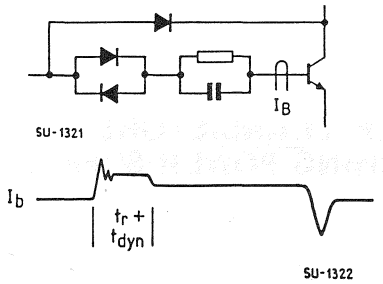
Fig. 4



quasi-saturation achieved and base current is diverted to the collector.

If there is a speed up circuit such as an RC network in the base circuit we see:

Fig. 5

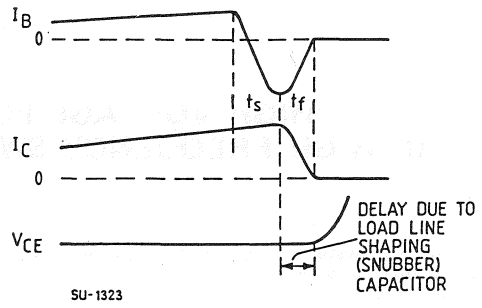


The speed up network gives an overshoot of base current and minimises the t_r and t_{dyn}.

Note that if the antisaturation network does not divert any base current the transistor has inadequate gain or the drive circuit needs adjustment to increase the available base drive. If the antisaturation network is not part of the design it should be removed before making further evaluations as it has the effect of improving the switching performance during turn-off.

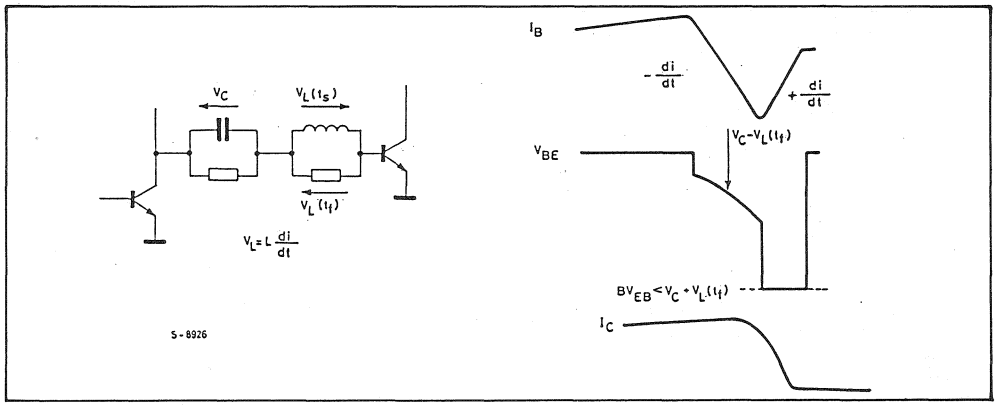
Looking at the turn-off we see:

Fig. 6



Note that the relationship of base and collector current during the fall time is not true if a base inductance is included which takes the base-emitter junction into reverse breakdown. Under these conditions the negative base current continues until the drive circuit's energy is exhausted. This type of circuit is similar to:

Fig. 7

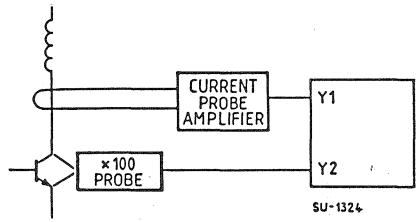


The voltage across the inductor tends to oppose the negative base bias during the storage time and in general the inductor increases storage time. The sign of di/dt changes when the fall time begins and so the voltage across the inductor reverses and can easily exceed the 10 to 15 volt breakdown of the base-emitter junction. This has the beneficial effect of minimising the current tail on high voltage transistors which are of the older and slower generations. Used with the faster types such as the SGS FASTSWITCH series this base drive technique does not produce an improvement in fall time and generally will degrade the storage time.

Beware of misleading measurements. With very fast power transistors such as the SGS FASTSWITCH series having fall times below 100ns the equipment is critical.

The current probe amplifier has a typical delay of 30 to 50ns more than the voltage probe, this makes cross over times at turn-off look worse and at turn on look better using a resistive load test.

Fig. 8



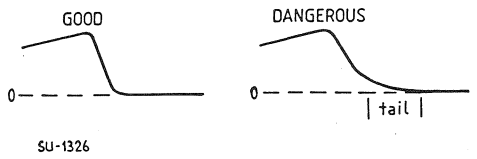
Often the falling edge appears unstable:

Fig. 9

The jitter on the pulse width can be avoided by triggering externally from the drive circuit 'turn-off pulse'.

Watch carefully for current 'tailing' at the end of the turn off period.

Fig. 10



Tailing is liable to cause failures of the power transistor due to going beyond the high voltage, low current RBSOA limit.

Often the heaviest stress on the power transistor is with maximum load and the AC line at the minimum specification for the unit. To evaluate the transistor stress run the supply in these conditions with the power transistor in free air, or on a small heatsink in > 150W applications, so that it gets hot.

Case temperatures of 80°C to 120°C are acceptable during these tests.

By reducing the snubber current limit resistor to 30% of its normal value the overshoot of I_C at turn-on can be seen and also the t_{dyn} can be evaluated. In the case of a capacitor below 470pF the resistor could be short circited. This test should be made with high line input and also checked with a 1 to 2Ω resistor in series with the base to limit the drive to the transistor.

Reduce the snubber capacitor to 70% of its normal value and check that both in high and low line conditions that at turn-off I_C reaches zero before the collector voltage reaches the $V_{CEO(sus)}$ rating of the transistor.

If a speed up RC network is used in the base circuit reduce the capacitor to half its normal value and verify that the switching, both turn-on & turn-off, is acceptable (even though it may be degraded).

If combining all these 'degredations' results in the power device still functioning within its absolute maximum ratings then one can be confident that, with normal spreads in values and transistor characteristics, the power switching stage will be reliable in worst case operation of the supply.